

# Dvts Apporach to Digital Cmos Circuits for Decreasing Total Power Consumption

Archanadevi.C, Vishnu Vardhan Rao.G,

**Abstract**— Power consumption of Modern Digital integrated circuits increasing with each generation which becomes a serious design issue. This paper proposed a generalized power tracking algorithm that reduces power directly by dynamic control of supply voltage and body bias. The DVTS algo-rithm-(Dynamic Voltage and threshold scaling algorithm) save the leakage power during active mode of the circuit. Total active power can be minimized by dynamically adjusting Vdd and Vth based on circuit operating conditions such as temperature, workload, and circuit architecture. The power saving method of DVTS is similar to that of the Dy-namic VDD Scaling (DVS) scheme, which adaptively changes the supply voltage depending on the current work-load of the system. For a digital circuit, it is possible to trade off dynamic and sub threshold leakage power by balancing between Vdd and Vth to maintain performance.

**Index Terms**— Dynamic voltage and threshold scaling (DVTS), leakage current control, low power, power optimum point, sleep transistor, variable body bias, and variable supply voltage.

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## 1 INTRODUCTION

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. In the past, the major concerns of the VLSI designer were area, performance, cost and reliability; power consideration was mostly of only secondary importance. In recent years, however, this has begun to change and, increasingly, power is being given comparable weight to area and speed considerations. Several factors have contributed to this trend. Perhaps the primary driving factor has been the remarkable success and growth of the class of personal computing devices (portable desktops, audio- and video-based multimedia products) and wireless communications systems (personal digital assistants and personal communicators) which demand high-speed computation and complex functionality with low power consumption.

Power dissipation has become an important objective in the design of digital circuits. There has been intense research over the past two decades on various aspects of compilation and synthesis for low power. Many architectural optimizations like re-configurable architectures, custom ASIC approaches, programmable multi-cores, *etc.* have been explored. Micro-architectural techniques like parallelism and pipelining, power and clock gating have become common place now. Circuit techniques for low voltage operation, standby current reduction, optimal gate sizing have also been explored and are available for use by a designer. Most of these optimization techniques are static techniques which are applied during design time. In the recent past, dynamic power management techniques have emerged, where the power consumption is continuously adjusted during run time of the system. Traditionally, Dynamic power management (DPM) is employed at operating system level to adjust the supply voltage for each power state. The supply voltage is conservatively margined to account for process and temperature variations.

These voltage margin increases with technology scaling due to larger process variations, rendering DPM less efficient. On the other hand, the hardware approach like dynamic voltage scaling (DVS) allows voltage to be scaled such that the actual delay of the chip instead of worst case delay meets the target performance. This enables more power savings as minimum possible voltage for target performance can be attained. In DVS the supply voltage is adjusted to meet the target delay using an on-chip delay monitor in a hardware feedback loop. Performance degradation is a direct consequence of supply voltage reduction. In order to maintain the required throughput, dynamic voltage scaling (DVS) systems are used to adjust the supply voltage according to throughput requirements. Though DVS very well manages the dynamic switching power, with shrinking feature size the static (leakage) power has increased exponentially which it cannot control. Particularly, at low activity levels, leakage power is dominant.

We present a Dynamic VTH Scaling (DVTS) scheme to save the leakage power during active mode of the circuit. Dynamic voltage and threshold scaling (DVTS) manages both dynamic and leakage powers by adjusting supply voltage and body bias voltage. The power saving strategy of DVTS is similar to that of the Dynamic VDD Scaling (DVS) scheme, which adaptively changes the supply voltage depending on the current workload of the system. Instead of adjusting the supply voltage, DVTS controls the threshold voltage by means of body bias control, in order to reduce the leakage power. The power saving potential of DVTS and its impact on dynamic and leakage power is applied to future technologies.

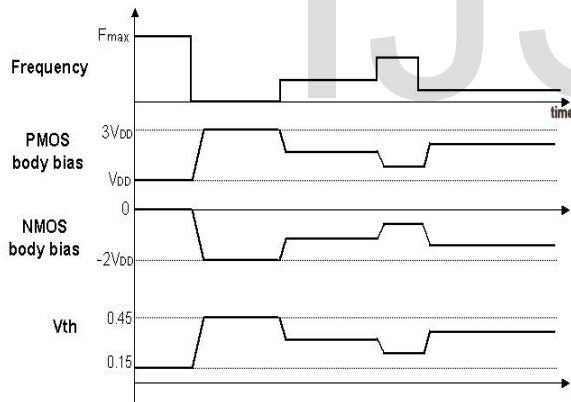
## 2 DYNAMIC VOLTAGE AND THRESHOLD SCALING

Dynamic voltage and threshold scaling (DVTS) manages both dynamic and leakage powers by adjusting supply voltage and body bias voltage. In digital circuits designed below 0.1  $\mu\text{m}$ , total power at any given performance can be opti-

mized by DVTS. DVTS has been successfully proven on silicon for low power high speed applications. The optimum power point varies strongly with activity and temperature. DVTS offers considerable power savings compared to DVS when leakage power is a large fraction of total power. The power savings increase with increasing logic depth. The moderate performance application-specific integrated circuit (ASIC) with long logic depth at low activity and/or high temperatures gain the most with DVTS.

## 2.1 Overview of Dvts

Dynamic VTH Scaling (DVTS) scheme for active leakage power reduction. Whenever there is a slack during computation, the VTH is adaptively changed to a higher value via changing the body bias voltage (VBB). This will deliver just enough amount of throughput required for the current workload. In order to examine the effectiveness of DVTS, comparisons between DVS and DVTS for current (0.25 $\mu$ m) and future (0.07 $\mu$ m) process generations are performed. A careful investigation on the advantages and disadvantages of DVTS over DVS is also made. A DVTS hardware that has a feedback loop consisting of a voltage controlled oscillator (VCO), charge pumps a feedback controller is proposed. The clock frequency of the system for a certain workload is determined by the operating system in run-time. The DVTS hardware tracks the optimal VTH for the given clock frequency by dynamically adjusting the VBB.



“Fig.1. Dynamic VTH scaling by adaptively changing the body bias”.

Fig.1 shows how the DVTS scheme adaptively controls the body bias to change the VTH. For a time period when the workload is less than the maximum, the operating system will recommend a lower clock frequency to the hardware. Then the DVTS hardware will increase the PMOS body bias and decrease the NMOS body bias to raise the VTH and reduce power dissipation. In cases when there is no workload at all, the VTH can be increased as much as the upper limit of VBB, to significantly save the standby leakage power. Reducing the clock frequency will proportionally reduce the total power. However, simply reducing the clock rate does not affect the energy consumed per operation. Whereas by scaling the supply voltage together with the frequency, we can gain

significant power savings. This is because the dynamic power dominates the total power. Scaling the threshold voltage instead of scaling the supply voltage saves mostly the leakage power. For 0.25 $\mu$ m technology where the leakage power is a minute portion of the total power, DVTS is less efficient than DVS in saving total power..

## 2.2 Modules of Dvts

### 2.2.1 VDD Controller

- Vdd is the power supply to the digital circuit. Vdd will be scaled according to power consumption and time delay. Maximum time delay will be set and between in that limits Vdd will be scaled.
- If Vdd goes below the minimum Vdd value Vdd value will be increased.

### 2.2.1 VBS Controller

- Vbs is the voltage between source and substrate. Vbs will effect threshold voltage. Vbs of the digital circuit will be varied to decrease the threshold voltage.
- In DVS only Vdd will be scaled to decrease total power consumption in dvts approach both Vdd and Vbs will be scaled to decrease total power consumption.

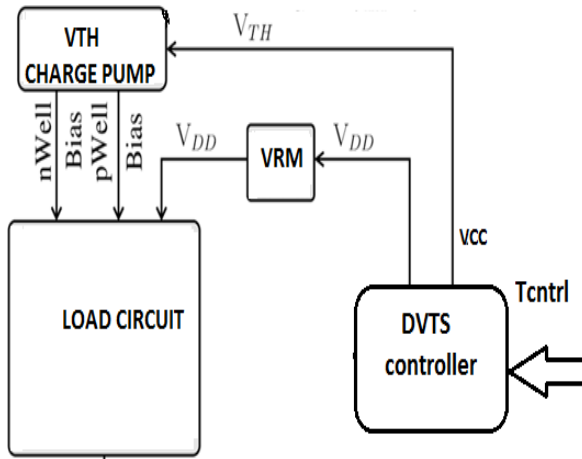
## 2.3 DVTS Scheme

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## 2.4 Dvts Controller

Fig.2 shows block diagram of close loop DVTS system. DVTS controller implements the proposed DVTS algorithm and controls the supply voltage regulator and well bias charge pump. Control signal generator (CSG) generates con-

control signals for power monitor when START signal is asserted. The proposed DVTS system is suited for load circuits where the rate of change in activity is gradual. DVTS controller implements the proposed DVTS algorithm and controls the supply voltage regulator and well bias charge pump. The drain of sleep transistor acts as a virtual ground node for the load circuit.



“Fig.2 Design Implementation Block Diagram”

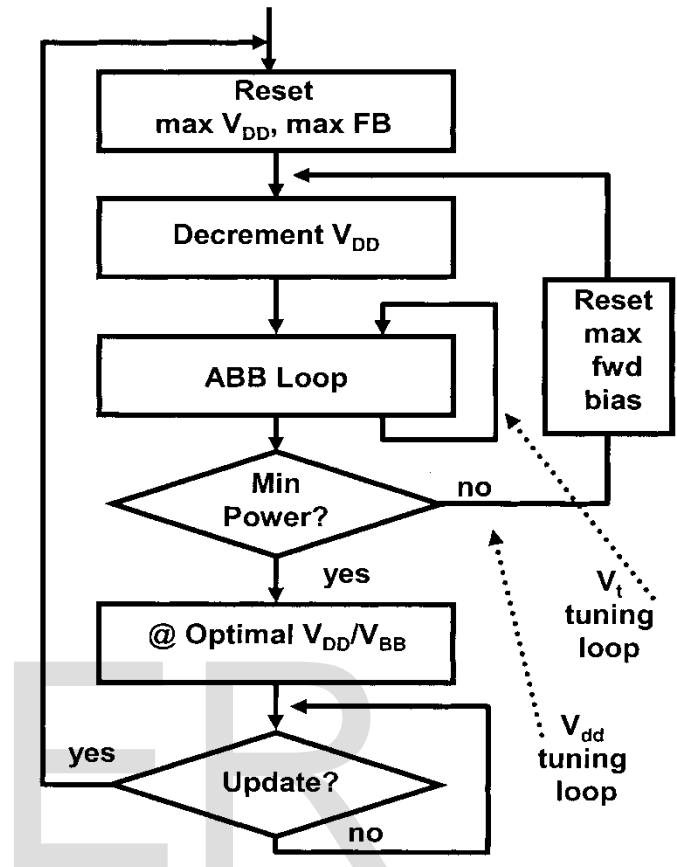
The power monitor processes virtual ground voltage to generate a 2 bit output that gives information on total power consumed by the load. Control signal generator (CSG) generates control signals for power monitor when START signal is asserted. The delay monitor measures whether performance of load circuit meets the target performance within tolerance limit. Delay monitor is implemented with a critical path replica circuit. The proposed DVTS system is suited for load circuits where the rate of change in activity is gradual. The maximum rate of change of activity that can be supported is discussed.

### 3 DVTS ALGORITHM

Fig.3.1 shows the flow chart of the proposed DVTS algorithm. The algorithm first sets the supply voltage to meet target performance, then adjust well potential to achieve minimum power. NWell bias and P Well bias are always tuned by same amount and hence DVTS control loop is essentially a 2-D control loop. To avoid oscillations, loop and loop are decoupled by tuning them independently. Initially maximum supply voltages and maximum forward bias are applied and the supply voltages are slowly lowered. At each step, the body bias is reset to maximum forward bias and locks to the target frequency to ensure that the chip stays functional. Once the minimum power point is detected, the bias values can be held in a register and the controller turned off. The loop can be reactivated whenever the workload changes, or periodically updated to reflect changes in

temperature or operating conditions. Because the ASB loop does not have to be constantly running, the overhead power consumption, which is already amortized across the whole chip, can be reduced even further. This ASB control loop is

completely self-contained and should lock to the true minimum power configuration taking into account all possible current paths



“Fig.3 (a) Flowchart for automatic V<sub>dd</sub> / V<sub>th</sub> optimization.”

This minimum will result in the physically lowest power consumption achievable by tweaking both and subject to the constraint that the chips satisfy a target frequency. Even for technologies where the theoretical limit is not yet achievable using body biasing techniques or in cases where excessive forward bias at low degrades performance, it is still possible to use this architecture to find the minimum physical power condition. The threshold voltage can be controlled by changing the body bias of the transistors and is called the adaptive body bias (ABB) technique. For fast silicon, reverse body bias is applied to increase threshold and reduce leakage, while for slow silicon, forward body bias is applied to reduce threshold and improve performance. Here the body bias adjustment is done sparingly as needed based on the chip’s process condition, and is not a continuous variable like the supply voltage. However the point of minimum power depends on the ratio of dynamic to leakage power, with the former modulated by the activity factor. For media applications, the activity factor can vary a lot across different applications and hence, the optimal settings for threshold and supply also vary. Analogous to table based DVS, a table based DVTS scheme has been proposed where for different activity factors, the corresponding supply and body bias values are stored in the look up table. The activity factors

are estimated for different applications off-line. During run-time, based on the application being run, the appropriate activity factor is used to consult the look up table to obtain the settings for supply and body bias, which will minimize power. Adaptive voltage and threshold scaling aims to arrive at the optimal voltage and threshold values at run time, by not only adapting to the process and temperature like in AVS, but also to the dynamically varying activity conditions.

#### 4 ADVANTAGES DVTS OVER DVS

##### No voltage level converters:

DVS or multiple VDD systems require a voltage level shifter whenever a low VDD signal is driving a high VDD receiver. Although the conventional level converters prevent the static power consumption, the dynamic power consumption is large enough to cancel out the power savings gained from supply voltage scaling. Since DVTS systems use the same supply voltage throughout the chip, no voltage level converters are required.

##### Simple hardware:

Charge pumps are a simple solution for boosting voltages. No external inductors are needed and power consumption is very low compared to buck converters, which are used for DVS systems. Charge pumps are used for our DVTS system to generate the body bias voltages

##### Less power loss charging/discharging internal nodes:

Transition energy wasted charging/discharging the VDD ground capacitance is the power overhead of the DVS scheme. For low-to-high and high-to-low transition of supply voltage, current is extracted or placed back to the power supply. Even though there is no computation during this cycle, transition energy is consumed. Since the supply voltage is fixed for DVTS, it has less transition energy loss while charging and discharging the internal nodes.

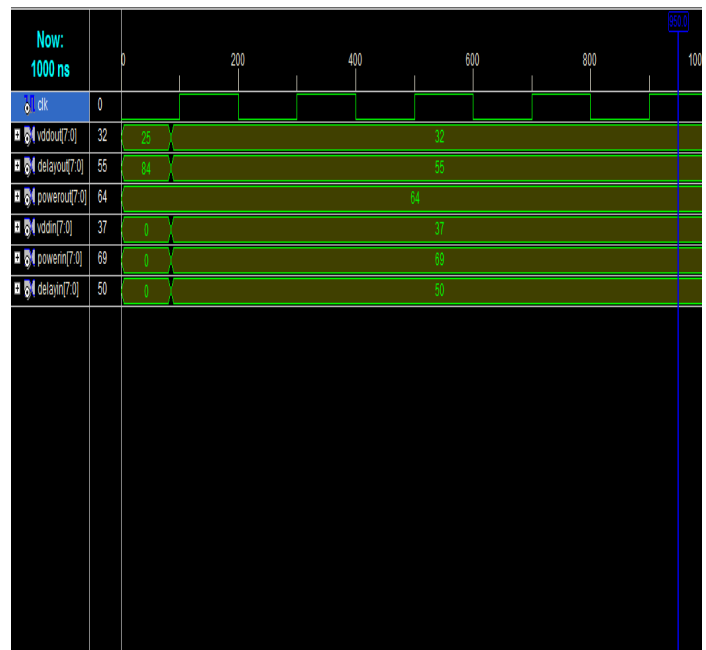
##### Improvement in noise immunity:

Signal integrity has become an important issue for deep sub micron devices as crosstalk noise becomes considerable. Increasing VTH for low workload periods in DVTS will help improve noise immunity, especially for noise-susceptible circuits such as domino logic and pulsed flip-flops.

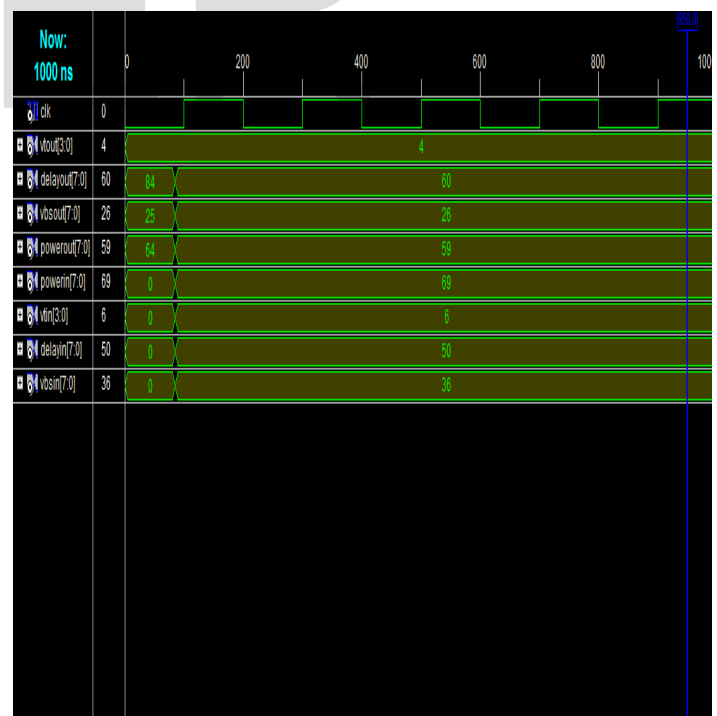
### 5 RESULTS AND DISCUSSION

To mitigate the active leakage problem, a Dynamic VTH Scaling (DVTS) scheme is presented. DVTS algorithm that can be studied and implemented for the design of VDD controller. VDD will be scaled and controlled according to the limits for the circuit. Power reduction technique can be applied to basic cmos circuits and the results for average power are analyzed. Ex. Inverter, NAND, NOR, multiplexer this idea can be extended to larger circuits in future

### 5.1 VDS and VBS controller results

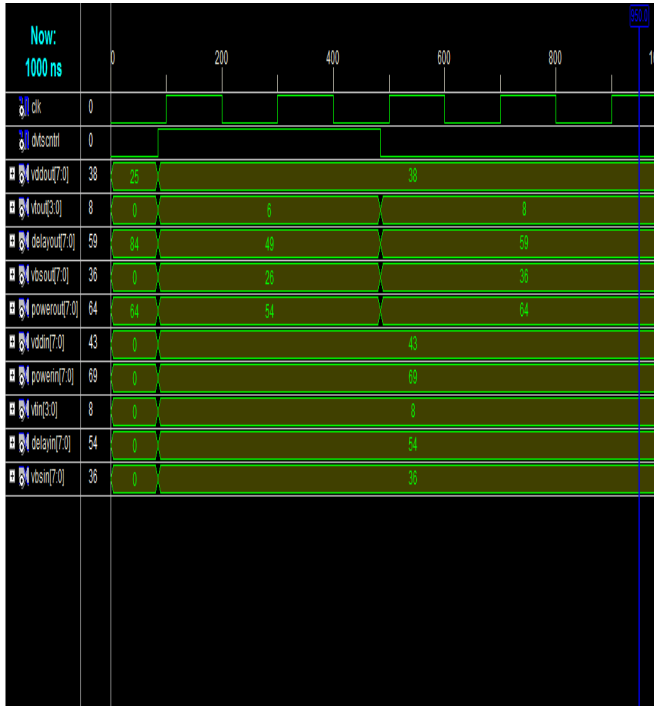


“Fig.5.1 VDD controller Graph results”

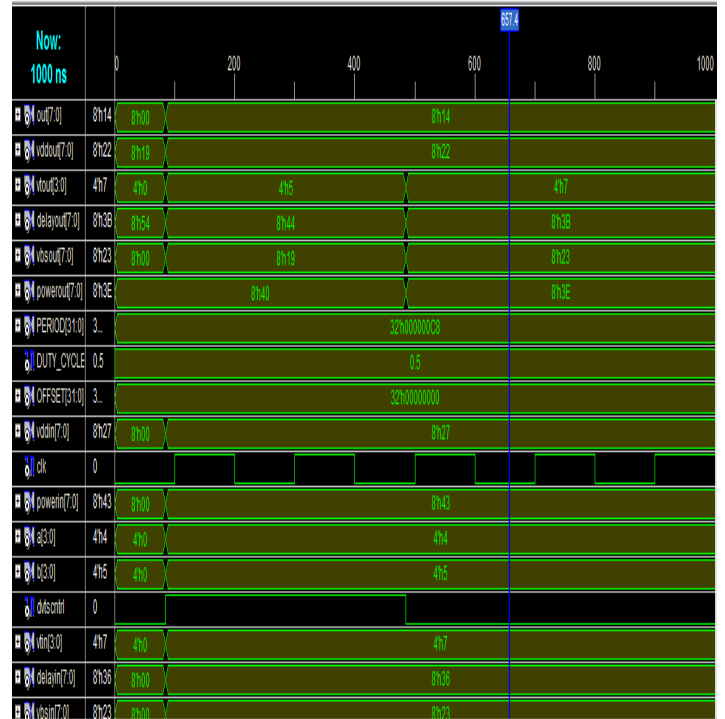


“Fig 5.2 VBS controller Graph results”

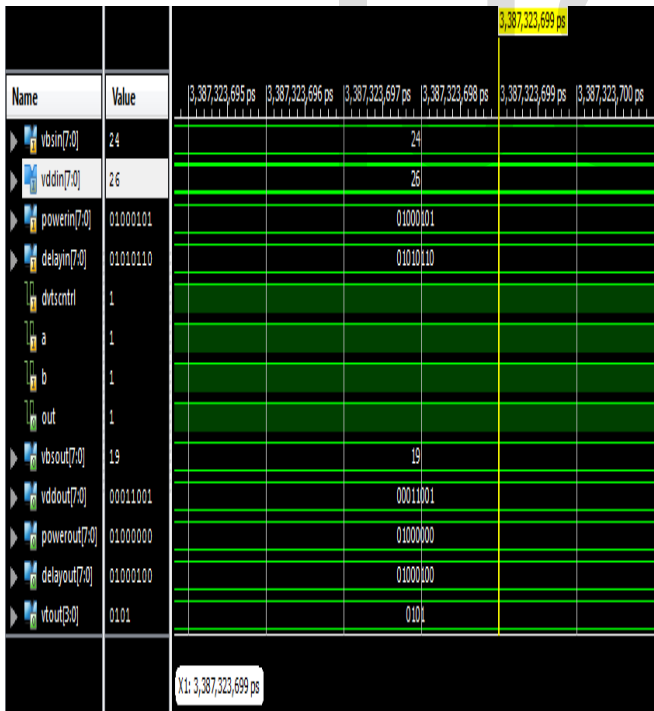
### 6 DVTS CONTROLLER RESULTS



“Fig 6.1 DVTS controller Graph results”



“Fig 6.3 Four Bit Multiplier Graph results”



“Fig 6.2 One Bit Multiplier Graph results”

## 7 Appendices



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